WHAT IS CLAIMED IS:

1. A method for controlling the amount of gate leakage in a semiconductor device, comprising:

placing a semiconductor substrate in a plasma chamber; and

subjecting a gate dielectric layer located over said semiconductor substrate to a gas mixture including argon and nitrogen under plasma conditions, wherein a flow rate of said argon ranges from about 1700 sccm to about 2200 sccm and a flow rate of said nitrogen ranges from about 40 sccm to about 200 sccm.

2. The method as recited in Claim 1 wherein said subjecting is conducted at a pressure ranging from about 700mT to about 1100 mT.

3. The method as recited in Claim 2 further including adjusting a flow rate of said argon and said nitrogen and a pressure of said plasma conditions to provide a desired gate leakage of said semiconductor device.

4. The method as recited in Claim 3 wherein said desired gate leakage is achieved while maintaining a target equivalent oxide thickness.

5. The method as recited in Claim 1 wherein a power of said plasma ranges from about 800 watts to about 1000 watts and a temperature of said semiconductor substrate ranges from about 300°C to about 500°C.

6. The method as recited in Claim 1 wherein subjecting is conducted in a microwave chamber and in a presence of oxygen.

7. The method as recited in Claim 1 wherein a flow of said argon is about 1950 sccm.

8. The method as recited in Claim 1 wherein a flow of said nitrogen is about 100 sccm.

9. The method as recited in Claim 1 wherein said subjecting results in a semiconductor device wherein a concentration of nitrogen within said gate dielectric layer ranges from about 5% to about 15% and an equivalent oxide thickness of said gate dielectric layer is about 1.25 nm and a gate leakage of said gate dielectric layer ranges from about 30 A/cm^2 to about 80 A/cm^2.

10. The method as recited in Claim 9 wherein said concentration of said nitrogen is about 11%.

11. A method of forming a gate dielectric in a plasma chamber, comprising:

placing a semiconductor substrate in a plasma chamber;

forming a gate dielectric layer over said semiconductor substrate;

subjecting said gate dielectric within said plasma chamber to a gas mixture including argon and nitrogen under plasma conditions, wherein a flow rate of said argon ranges from about 1700 sccm to about 2200 sccm and a flow rate of said nitrogen ranges from about 40 sccm to about 200 sccm and under high pressure.

12. The method as recited in Claim 11 wherein said high pressure ranges from about 700mT to about 11000 mT.

13. The method as recited in Claim 11 further including adjusting a flow rate of said argon and said nitrogen and a pressure of said plasma conditions to provide a desired gate leakage of said semiconductor device, wherein said desired gate leakage is achieved within a targeted equivalent oxide thickness and in a presence of oxygen.

14. The method as recited in Claim 11 wherein a power of said

plasma ranges from about 800 watts to about 1400 watts and a temperature of said semiconductor substrate ranges from about 300°C to about 500°C.

15. The method as recited in Claim 11 wherein a flow rate of said argon is about 1950 sccm and a flow of said nitrogen is about 100 sccm.

16. The method as recited in Claim 11 further including:

forming a gate layer over said gate dielectric layer;

patterning said gate layer and said gate dielectric layer into a plurality of transistor gates;

forming source/drains in well regions associated with each of said plurality of said transistor gates, said well region being located in said semiconductor substrate and between isolations regions located between said transistor gates;

forming dielectric layers over said transistor gates; and

forming interconnects in and between said dielectric layers to interconnect said transistor gates to form an operative integrated circuit.

17. A semiconductor device having a predetermined gate leakage, comprising;

a semiconductor substrate; and

a gate dielectric layer located over said semiconductor substrate, said gate dielectric layer having a concentration of nitrogen therein that ranges from about 5% to about 15% and an equivalent oxide thickness that ranges from about 1.0 nm to about 1.5 nm and wherein a gate leakage of said gate dielectric layer is less than about 100 A/cm^2.

18. The semiconductor device as recited in Claim 17 wherein a concentration of said nitrogen is about 11% and said gate leakage ranges from about 30 A/cm^2 to 40 A/cm^2.

19. The semiconductor device as recited in Claim 17 wherein said gate leakage ranges from about 30 A/cm^2 to about 80 A/cm^2.

20. The semiconductor device as recited in Claim 17 wherein a concentration of said nitrogen is about 8% and said gate leakage is about 80 A/cm^2.